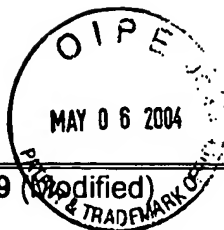


Form PTO-1449 (Modified)				Atty Docket No.: 03692.P054D2		Serial No.: 10/647,925	
List of Patents and Publications Statement (Use several sheets if necessary)				Applicants: Disney, D. Filing Date: August 26, 2003			
REFERENCE DESIGNATION				U.S. PATENT DOCUMENTS			
Exam. Initial		Date	Document Number	Name	Class	Sub- Class	Filing Date
FOREIGN PATENT DOCUMENTS							
No.		Document No.	Date	Country	Name	Class	Sub- Class
Loke		JP 6-224426	08/12/94	Japan	Uno		English
Loke		DE 43 09 764	09/29/94	Germany	Tihanyi, et al.		
Loke		JP 56-38867	04/14/81	Japan	Okabe, T., et al.		English
Loke		JP 57-10975	01/20/82	Japan	Sanyo		English
Loke		JP 57-12557	01/22/82	Japan	Tanaka, et al.		English
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OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)							
Loke		"International Electron Devices Meeting 1979- Washington, D.C, Dec. 3-4-5," Sponsored by Electron Devices Society of IEEE, Pages 238-241.					
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Examiner Loke				Date Considered 6/29/04			
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							



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FOREIGN PATENT DOCUMENTS								
No.		Document No.	Date	Country	Name	Class	Sub-Class	Trans-lation
Loke		JP 3-211771	09/17/91	Japan	Toshiba			English
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No.		Document No.	Date	Country	Name	Class	Sub-Class
OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)							
Loke		"High Performance 600 V Smart Power Technology Based on Thin Layer Silicon-on-Insulator," T. Letavic, et al., Phillips Electronics North America Corp., 4 Pages.					
Loke		"Modern Semiconductor Device Physics," S. M. Sze, John Wiley & Sons, 1998, Chapter 4, Pages 203-206.					
Loke		"Modeling Optimization of Lateral High Voltage IC Devices to Minimize 3-D Effects," H. Yilmaz, R&D Engineering, GE Corp., NC, Pages 290-297.					
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